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09/417,034	10/12/1999	ANDREW W. KITTROSS	TER99-01	6903

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EXAMINER
WHITTINGTON, ANTHONY T

ART UNIT	PAPER NUMBER
2133	10

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/417,034	KITTROSS ET AL.	
	Examiner	Art Unit	
	Anthony T Whittington	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,and 4-24* is/are rejected.

7)☒ Claim(s) *3 and 25-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Preliminary Matters

The examiner has considered the all the references in the PTO-1449 form, which is now signed and will be returned in the next Office Action.

Drawings

The corrected or substitute drawings were received on 7-30-01. The examiner accepts these drawings.

Specification

The examiner accepts the amendment by the applicant to cure the minor informality.

Claims 3 and 25-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 3, the prior art of record neither singularly nor in combination teaches the limitation: "a second test element which defines a second test operation that provides a second result which is based on the first result."

Regarding claims 25,28 and 29, the prior art of record neither singularly nor in combination teaches to the newly added limitation: "obtains the first test result generated ...and (ii) generates a second test result based on the first test result."

Regarding claim 26, the prior art of record neither singularly nor in combination teaches to the newly added limitation: "test procedure is configured to direct the processor to the first and second test elements to perform a mixed signal test based on the first and second test elements."

Regarding claim 27, the prior art of record neither singularly nor in combination teaches to the newly added limitation: "test element defines instructions for only a partial device testing task."

Response to Arguments

Applicant's argument filed 2-19-03 have been fully considered but they are not persuasive.

As per claims 1-8:

The examiner has reconsidered the claims and concluded that the prior art of the record teaches the claimed invention as earlier presented in the first office action (See paper 7). The applicant contends that Noble does not teach a processor with the limitations: "(i) providing a series of instruction based on a test procedure defining a device testing task, and (ii) control the test interface based on the provided series of instructions in order to test the device with a test procedure that includes multiple test elements, programmable input variables, and test elements that define instruction. However, Noble does teach element (i) in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus ...or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs (series of instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests".

Noble also teaches all of the parts of element (ii). In column 1, lines 25-26: "CPU ...control functions for the tester (control the test interface)". In column 16, lines 11-35, Noble states: "[processor]...database of test elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation). For the sake of argument, a database by definition is a usually large collection of data organized especially for rapid search and retrieval (as by a computer) as found in the Webster dictionary. Therefore, a large collection of test elements is construed as multiple test elements. Test elements posses the characteristic inherently as being defined by instruction. In light of the clarification that Noble does teach all the elements of claim 1, claims 2-8 remain rejected under the same grounds as before (See paper 7).

The examiner is not clear with the argument that involves Le in regards to claim 1 to determine if patentably distinct over the prior art. Claim 1 is rejected under 102(e) anticipation with respect to MPEP 2131. As stated in MPEP 2131, the reference must teach every element of the claim to anticipate a claim as seen with the Noble reference for claim 1. The Le reference has no bearing on claim 1. Regardless, if Le's mixed signal device teaches or teaches away from Noble's system is not considered with an anticipatory rejection (See MPEP 2131.05). As stated in MPEP 2131.05, "arguments that the alleged anticipatory... prior art teaches away are not germane to rejection under section 102."

As per claims 9 and 17, the examiner uses the same reasoning since these claims are directed in similar scope as the methods associated with claim 1. See the arguments above for

further explanation. As stated above for similar reasons as claim 1 with respect to dependent claims from claim 1, claims 10-16 and 18-19 remain rejected under the same grounds of rejection (See paper 7).

As per claims 20-23, Noble teaches test elements in column 16, lines 49-50: "read test program elements (test elements) from the database of test program elements". Therefore, the rejection of claims 20,21,22, and 23 under 35 USC 102(e) will be maintained.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 24 is rejected under 35 U.S.C. 102(e) as being anticipated by Noble (U.S 5,892,949).

As per claim 24, Noble teaches each test element of a set of test elements within the test procedure in column 16, lines 11-35, Noble states: "[processor]...database of test elements (multiple test elements)".

The previous rejection is maintained. The following is the previous rejection:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims1-6,8-14,16-18,20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Noble (U.S. 5,892,949).

As per claim 1, Noble teaches a system for testing a device that is equivalent to the instant application. Noble teaches the first element of claim 1, memory (112, Fig.1) having a test application stored therein, in column 3, line 51. Noble teaches the second element of claim 1, a

test interface (hardware interface, part of the tester) to connect to a device in Figure 2. Noble teaches the third element of claim 1, processor (111) coupled to the memory(112) and the test interface(110), in Figure 1 and in column 3,lines 50-52. Noble teaches the fourth element of claim 1, processor being configured to operate with the test application in column 3, lines 49-51. Noble states in column 3, line 49-51: "under the control of a CPU executing a test program (application) stored in a random access memory." Noble teaches the fourth element (i) of claim1, [processor] provide a series of instructions based on a test procedure defining a device testing task, test procedure including multiple test elements, test element defining instructions, programmable input variables that direct the processor to perform a particular test, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus....or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs(series of instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation). Noble teaches the fourth element (ii) of claim1, [processor] control the test interface (tester) based on the provided series of instructions in order to test the device, column 16, lines 15-18.

As per claims 2 and 10, Noble teaches the use of an I/O device coupled to the processor that aides the processor in operating the test application to provide a graphical user interface to the user is found in column 3, lines 50-56. Noble states: "CPU may communicate with.... a computer (containing I/O devices such as a display, mice, etc.). Noble teaches the first element of claims 2 and 10, combining test elements from a test element database to form the test procedure, in column 4, lines 35-60. Noble states: "Tools communicate through...ORB to objects (test elements) that make up the test program (combination to make up procedure). These objects (test elements) are stored ...in an object database (ODB)". Noble teaches the second element of claims 2 and 10, programmable input variables of each test element forming the test procedure to initial values in column 13, lines 40-55. Noble teaches of a FTest procedure, where each object (test element) has variables that can be inputted. Noble teaches the third element of claims 2 and 10, indicating an operating order for the test elements, in column 4, lines 33-67. Noble teaches various objects (test elements) such as the Ftest and shows the order of operation of each. Noble teaches the fourth element of claims 2 and 10, storing the test procedure within memory, in column 3, line 51. Noble states: "a test program stored in a random access memory".

As per claim 4, Noble teaches of a test procedure that is a nested test procedure that is nested within another test procedure that is equivalent to the instant application in column 13, lines 1-67. Noble teaches in column 13, lines 34-60 of an interface (test procedure) with a nested loop inside of it and is a nested loop.

As per claims 5 and 6, Noble teaches the first element of claim 5 and 6, processor includes multiple processing units that are associated with respective multiple devices, in column

2, lines 42-54. Noble states: " embedded computer (processor), second computer, and the third computer are the same computer or different computers". Noble teaches the second element of claims 5 and 6, each processing unit is configured to control a respective portion of the test interface, in column 2, lines 30 –43. Noble states: " first computer for use of the user...POEM running on the second computer...ORB running on third computer". Noble teaches the third element of claim 5 and 6, providing a series of instructions to test the respective multiple devices in parallel, in column 3, lines 14-17. Noble states: "architecture supports... [testing] different parts of the same test program in parallel. ...users working remotely." The user defines if the test interface is single instance or a series of instructions at the computer terminal by the user working remotely.

As per claim 8, Noble teaches the first element of claim 8, a processor analyzing the test procedure to identify the which programmable input variables of the test elements of the test procedure require initial values, in column 11, line 1 –25. Noble states: " initializing appropriate storage...creating a persistent object (analyze the test procedure)...changing the data in...persistent object (programming input variables of test element that require initial values) . Noble teaches the second element of claim 8, a processor creating a graphical user interface component which prompts a user to provide the required initial values to initialize the identified programmable input variables, column 13, lines 1-67. Noble teaches an example of graphical user interface component that prompts the user for initialization of parameters, or programmable input variables.

As per claim 9, Noble teaches the first element of claim 9, obtaining a test procedure which defines a device testing task, in column 3,line 65-column 4, line 7. Noble states: " select a test program (obtaining a test procedure)" Noble teaches the second and third elements of claim 9, test procedure including multiple test elements, test element defining instructions, programmable input variables that direct the processor to perform a particular test and [processor] provide a series of instructions based on a test procedure, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus....or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs(series of instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation).. Noble teaches the fourth element of claim 9, [processor] control the test interface (tester) based on the provided series of instructions in order to test the device, column 16, lines 15-18.

As per claim 11, Noble teaches the step of providing instructions that takes a first test element, which defines instructions to the processor and performs a first test operation in column 5, lines 1- 37. Noble states in column5, lines1-4: "POEM (first test operation) , implementing all of the test objects." Noble teaches of a test procedure that takes a second test element, which defines instructions to the processor and performs a second test operation based on first result in

column 5, lines 5-15. Noble states: "ORA (second test operation) to which is passed an object reference (test element with first operation to make a reference) corresponding synthetic test program object in POEM (first test operation)".

As per claim 12 and 18, Noble teaches the test procedure that is a nested test procedure that is nested within another test procedure that is where the step includes providing instructions directing the processor to perform the device testing task when providing instructions based on the other test procedure in column 13, lines 1-67. Noble teaches in column 13, lines 34-60 of an interface (test procedure) with a nested loop inside of it and is a nested loop.

As per claim 13 and 14, Noble teaches of a test interface including multiple processing units that are associated with respective multiple devices, in column 2, lines 42-54. Noble states: " embedded computer (processor), second computer, and the third computer are the same computer or different computers". Noble teaches each processing unit is configured to control a respective portion of the test interface, in column 2, lines 30 –43. Noble states: " first computer for use of the user...POEM running on the second computer...ORB running on third computer". Noble teaches the test interface based on instructions defined by a "single instance" of the test procedure to test the respective multiple devices in parallel, in column 3, lines 14-17. Noble states: "architecture supports... [testing] different parts of the same test program in parallel...users working remotely." The user defines if the test interface is single instance or a series of instructions at the computer terminal by the user working remotely.

As per claim 16, Noble teaches the first element of claim 16, a processor analyzing the test procedure to identify the which programmable input variables of the test elements of the test

procedure require initial values, in column 11, line 1 –25. Noble states: " initializing appropriate storage...creating a persistent object (analyze the test procedure)...changing the data in...persistent object (programming input variables of test element that require initial values) . Noble teaches the second element of claim 16, a processor creating a graphical user interface component which prompts a user to provide the required initial values to initialize the identified programmable input variables, column 13, lines 1-67. Noble teaches an example of graphical user interface component that prompts the user for initialization of parameters, or programmable input variables.

As per claim 17, Noble teaches a method for providing a test procedure that is the first element of claim 17, combining test elements from a test element database to form the test procedure, in column 4, lines 35-60. Noble states: "Tools communicate through...ORB to objects(test elements) that make up the test program(combination to make up procedure). These objects (test elements) are stored ...in an object database (ODB)." Noble teaches the sub elements of claim 17, test procedure including multiple test elements, test element defining instructions, programmable input variables that direct the processor to perform a particular test and [processor] provide a series of instructions based on a test procedure, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus....or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs(series of instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test elements (multiple test elements)...being

programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation).. Noble teaches the third element of claim 17, setting a portion of programmable input variables of each test element forming the test procedure to initial values in column 13, lines 40-55. Noble teaches of a FTest procedure, where each object (test element) has variables that can be inputted. Noble teaches the fourth element of claim 17, indicating an operating order for the test elements, in column 4, lines 33-67. Noble teaches various objects (test elements) such as the FTest and shows the order of operation of each. Noble teaches the fifth element of claim 17, storing the test procedure within memory, in column 3, line 51. Noble states: "a test program stored in a random access memory".

As per claim 20, Noble teaches in column 3, line 49-57, a computer program product with a computer readable medium having instructions stored thereon that is equivalent to the instant application. Noble teaches the first element of claim 20, obtaining a test procedure which defines a device testing task, in column 3,line 65-column 4, line 7. Noble states: " select a test program (obtaining a test procedure)" Noble teaches the second and third elements of claim 20, test procedure including multiple test elements, test element defining instructions, programmable input variables that direct the processor to perform a particular test and [processor] provide a series of instructions based on a test procedure, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus....or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs(series of instructions based on a test procedure defining a device

taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation).. Noble teaches the fourth element of claim 20, [processor] control the test interface (tester) based on the provided series of instructions in order to test the device, column 16, lines 15-18.

As per claim 21, Noble teaches in column 3, line 49-57, a computer program product with a computer readable medium having instructions stored thereon that is equivalent to the instant application. Noble teaches a data process device to perform steps of a test procedure where the first element of claim 21, combining test elements from a test element database to form the test procedure, is found in column 4, lines 35-60. Noble states: "Tools communicate through...ORB to objects(test elements) that make up the test program(combination to make up procedure). These objects (test elements) are stored ...in an object database (ODB)." Noble teaches the sub elements of claim 21, test procedure including multiple test elements, test element defining instructions, programmable input variables that direct the processor to perform a particular test and [processor] provide a series of instructions based on a test procedure, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus....or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs(series of

instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation).. Noble teaches the third element of claim 21, setting a portion of programmable input variables of each test element forming the test procedure to initial values in column 13, lines 40-55. Noble teaches of a FTest procedure, where each object (test element) has variables that can be inputted. Noble teaches the fourth element of claim 21, indicating an operating order for the test elements, in column 4, lines 33-67. Noble teaches various objects (test elements) such as the FTest and shows the order of operation of each. Noble teaches the fifth element of claim 21, storing the test procedure within memory, in column 3, line 51. Noble states: "a test program stored in a random access memory".

As per claim 22, Noble teaches an automatic test system having a computer readable memory that is equivalent to the instant application. Noble teaches a test procedure (computer program) including multiple test elements, each test element having user programmable input values, test element configures to direct the automatic test system to perform a test method, and multiple test procedures, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus....or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs(series of instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test

elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation).. Noble teaches the first and second sub elements of claim 22, multiple test elements and indicating an operating order for the test elements, in column 4, lines 33-67. Noble teaches various objects (test elements) such as the FTest and shows the order of operation of each. Noble teaches the last sub element of claim 22, setting a portion of programmable input variables of each test element forming the test procedure to initial values in column 13, lines 40-55. Noble teaches of a FTest procedure, where each object (test element) has variables that can be inputted.

As per claim 23, Noble teaches a method of programming an automatic test system that is equivalent to the instant application. Noble teaches in column 3, lines 14-16 and column 3, line 58-column 4, line 22 all the elements of claim 23. Noble teaches the first element of claim 23, providing a test development environment with a user actuated tool to select a test element from a set of test elements and test element data entry area displaying data entry fields. Noble states: " architecture supports development (development environment)....software tester architecture include a user interface(displaying data entry fields)...initializes the user interface ...requested by the user...Selection Tool... select a test program(test element, objects are test programs also column 4, line27-30) from a program database." Noble teaches the second element of claim 23, selecting a first test element from the set of test elements, in column 4, lines1-2. Noble teaches the third element of claim 23, entering data in the data entry for the selected test element, in column 4, lines 3-7. Noble states: " specify (entering) a sequence". Noble teaches the fourth and

fifth elements of claim 23, selecting and entering data for at least one additional test element, in column 4, lines 5-7. Noble state: "user select timing, patterns (collection of vectors) and levels of functional tests." Noble teaches the ability to select and modify various characteristics of additional test elements, which is equivalent to the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 7,15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble in view of Le (U.S. 6,353,904).

As per claim 7, Noble substantially teaches all the elements of claim 1. Noble teaches the first element of claim 1, memory (112, Fig.1) having a test application stored therein, in column 3, line 51. Noble teaches the second element of claim 1, a test interface (hardware interface, part of the tester) to connect to a device in Figure 2. Noble teaches the third element of claim 1,

processor (111) coupled to the memory (112) and the test interface (110), in Figure 1 and in column 3,lines 50-52. Noble teaches the fourth element of claim 1, processor being configured to operate with the test application in column 3, line 49-51. Noble states in column 3, line 49-51: "under the control of a CPU executing a test program (application) stored in a random access memory." Noble teaches the fourth element (i) of claim1, [processor] provide a series of instructions based on a test procedure defining a device testing task, test procedure including multiple test elements, test defining instructions, programmable input variables that direct the processor to perform a particular test, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus.... or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs (series of instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation). Noble teaches the fourth element (ii) of claim1, [processor] control the test interface (tester) based on the provided series of instructions in order to test the device, column 16, lines 15-18. Noble does not explicitly disclose a except for a mixed signal device where the first test element defines instructions for the processor to perform an analog signal test operation and a second test element defines instructions for the processor to perform a digital signal test operation.

However Le, in analogous art, teaches in column 2, lines 30-50 of a mixed signal device performing analog and digital test operations in automatic test equipment.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Noble's system by substituting test signal device with the mixed signal device. This modification would been obvious to a person having ordinary skill in the art because it would reduce any prolonged testing processes unnecessarily extending the product development cycle and increases development cost as suggested by Le in column 1,line 51-column 2, line 6.

As per claim 15, Noble substantially teaches all the elements of claim 1. Noble teaches the first element of claim 1, memory (112, Fig.1) having a test application stored therein, in column 3, line 51. Noble teaches the second element of claim 1, a test interface (hardware interface, part of the tester) to connect to a device in Figure 2. Noble teaches the third element of claim 1, processor (111) coupled to the memory (112) and the test interface (110), in Figure 1 and in column 3,lines 50-52. Noble teaches the fourth element of claim 1, processor being configured to operate with the test application in column 3, line 49-51. Noble states in column 3, line 49-51: "under the control of a CPU executing a test program (application) stored in a random access memory." Noble teaches the fourth element (i) of claim1, [processor] provide a series of instructions based on a test procedure defining a device testing task, test procedure including multiple test elements, test defining instructions, programmable input variables that direct the processor to perform a particular test, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus.... or

network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs (series of instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation). Noble teaches the fourth element (ii) of claim1, [processor] control the test interface (tester) based on the provided series of instructions in order to test the device, column 16, lines 15-18. Noble does not explicitly disclose a except for a mixed signal device where the first test element defines instructions for the processor to perform an analog signal test operation and a second test element defines instructions for the processor to perform a digital signal test operation.

However Le, in analogous art, teaches in column 2, lines 30-50 of a mixed signal device performing analog and digital test operations in automatic test equipment.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Noble's system by substituting test signal device with the mixed signal device. This modification would been obvious to a person having ordinary skill in the art because it would reduce any prolonged testing processes unnecessarily extending the product development cycle and increases development cost as suggested by Le in column 1,line 51-column 2, line 6.

As per claim 19, Noble substantially teaches all the elements of claim 1. Noble teaches the first element of claim 1, memory (112, Fig.1) having a test application stored therein, in column 3, line 51. Noble teaches the second element of claim 1, a test interface (hardware

interface, part of the tester) to connect to a device in Figure 2. Noble teaches the third element of claim 1, processor (111) coupled to the memory (112) and the test interface (110), in Figure 1 and in column 3,lines 50-52. Noble teaches the fourth element of claim 1, processor being configured to operate with the test application in column 3, line 49-51. Noble states in column 3, line 49-51: "under the control of a CPU executing a test program (application) stored in a random access memory." Noble teaches the fourth element (i) of claim1, [processor] provide a series of instructions based on a test procedure defining a device testing task, test procedure including multiple test elements, test defining instructions, programmable input variables that direct the processor to perform a particular test, in column 3, line 50 - column 4, line 23 and column 16, lines 11-35. Noble states in column 3, line 50 - column 4, line 23: " CPU may communicate with...computer, such as a single user workstation...connected by a bus.... or network... tester may be connected ...on a network...[processor] provides the user...managing and running test programs (series of instructions based on a test procedure defining a device taking task)...allows the user to specify a sequence of tests. Noble states in column 16, lines 11-35: "[processor]...database of test elements (multiple test elements)...being programmed to provide test program elements to the tester (test elements defining instructions and programmable input variables that direct the processor to perform a particular test operation). Noble teaches the fourth element (ii) of claim1, [processor] control the test interface (tester) based on the provided series of instructions in order to test the device, column 16, lines 15-18. Noble does not explicitly disclose a except for a mixed signal device where the first test element defines instructions for the processor to perform an analog signal test operation and a second test element defines instructions for the processor to perform a digital signal test operation.

However Le, in analogous art, teaches in column 2, lines 30-50 of a mixed signal device performing analog and digital test operations in automatic test equipment.

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Noble's system by substituting test signal device with the mixed signal device. This modification would been obvious to a person having ordinary skill in the art because it would reduce any prolonged testing processes unnecessarily extending the product development cycle and increases development cost as suggested by Le in column 1,line 51-column 2, line 6.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of art with respect to automatic test equipment in general:

U.S. Pat No.6,205,407 to Testa et al.

U.S. Pat No.5,968,192 to Kornachuk et al.

U.S. Pat No. 5,828,674 to Proskauer

U.S. Pat No. 6,128,759 to Hansen

U.S. Pat No. 5,668,745 to Day

U.S. Pat No. 5,794,007 to Arrigotti et al.

U.S. Pat No. 5,913,022 to Tinaztepe et al.

U.S. Pat No. 6,249,893 to Rajsuman et al.

U.S. Pat No. 6,408,412 to Rajsuman

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anthony T Whittington whose telephone number is 703-306-5617. The examiner can normally be reached on Monday-Friday 7:30a.m.-4:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

A.W.
March 31, 2003

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100